Census Transform Based Stereo Matching Accelerator

Hyeon-Sik Son, Kyeong-ryeol Bae, Seung-Ho Ok and Byungin Moon
School of Electronics Engineering
Kyungpook National University, Daegu, Korea
{soc_shs1984, puris1, wintiger}@ee.knu.ac.kr, bihmoon@knu.ac.kr

I. INTRODUCTION

3D vision processing is a core technology variously applied to intelligent robot vision systems, autonomous vehicle systems, 3D broadcast systems, mobile devices, etc. Most recent researches have been focused on the development of algorithm-centric vision systems based on the CPU or the GPU. There are some researches and developments for the implementation of hardware accelerators of 3D vision processing, but they are only about production of depth maps using FPGA devices which have constraints in cost and performance. On the other hand, there are few researches and developments for ASIC implementation of 3D vision processing. So, we developed a 3D visual information processing ASIC for low-power and small-area implementation.

II. DESCRIPTION

A. *Description System Architecture*

Fig. 1 shows the block diagram of the proposed 3D vision processing module, which consists of three blocks. The Pre-Processing block produces noise-removed images and edge information for the generation of reliable 3D depth maps. The Depth Extraction block produces 3D depth maps and depth-edge maps using Census transform algorithm[1] and disparity diffusion algorithm[2]. Finally, the 3D depth maps and depth-edge maps are de-noised by the Post-Processing block. These 3D depth maps and depth-edge maps are used for the extraction of distance and object information, respectively.

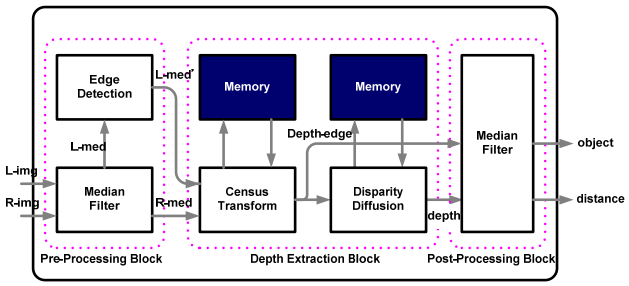

Fig. 1. Block diagram of the 3D vision processing ASIC.

B. *Design and Implemention*

The proposed 3D vision processing module was described and designed with Verilog HDL and verified by FPGA implementation. The test images of the Middlebury image sets [3] were used for this FPGA verification.

III. CHIP IMPLEMENTAION AND RESULTS

The 3D vision processing module verified by FPGA implementation was implemented in an ASIC through IDEC MPW with M/H 0.18 μm technology. Table 1 shows the detailed specifications of the 3D vision processing ASIC, and Fig. 2 shows its layout and package.

Specifications	
Gate count	560,000
Frequncy	26.6 MHz
SRAM	44 SRAMSs of 752 × 8
die size	4.5 mm × 4 mm
Package	LQFP 208

Table 1. Chip specifications.

Fig. 2. 3D vision processing ASIC.

REFERENCE

[1] S. Jin, J. Cho, X. D. Pham, K. M. Lee, S. –K. Park, M. Kim, and J. W. Jeon, "FPGA Design and Implementation of a Real-Time Stereo Vision System," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 20, no. 1, pp.15-26, Jan. 2010.

[2] S. Lee, N. Cho, and J. Park, "Disparity Estimation Using Color Coherence and Stochastic Diffusion," *Proc. 2004 International Conference on Image Processing*, vol. 2, pp. 1373-1376, Singapore, Oct. 2004.

[3] Middlebury Stereo Vision Page, http://vision.middlebury.edu/stereo/.

This work was supported by the IDEC.